

Brendan Lynskey

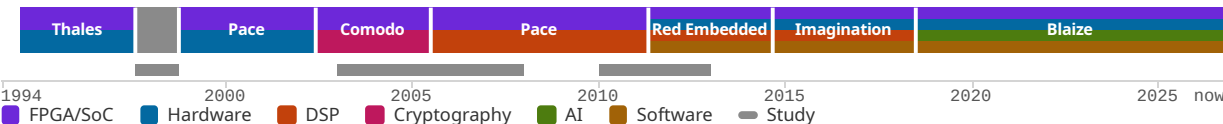
Experienced engineer working in AI systems (LLMs, agents, MCP, Python) with a background in FPGA, DSP, hardware and power.

Leeds, UK [linkedin.com/in/brendan-lynskey-a891705](https://www.linkedin.com/in/brendan-lynskey-a891705) github.com/BrendanJamesLynskey brendan-lynskey.vercel.app/

PROFILE

Engineer with over 25 years' experience across hardware, FPGA, SoC, DSP and software. Much of it designing and verifying FPGA or SoC systems (packet switching, high-speed serial links, cable modem PHY/MAC, CPU debug, broadcast video, cryptography), then board-level hardware for AI accelerators at Blaize: power delivery, signal integrity and DDR. For the last two years almost entirely software, mainly Python, building agentic AI systems with LangGraph and MCP; Claude Code every day. Keen to work where a hardware background counts, such as new compute architectures.

TIMELINE



EXPERIENCE

July 2018 – present

Staff Engineer · Blaize (formerly Thinci)

Leeds ● FPGA/SoC ● Hardware ● AI ● Software

Blaize makes energy-efficient SoCs for machine learning and computer vision. Dual role: software/AI engineering and hardware systems engineering.

- Building an agentic analytics system in Python with LangGraph, MCP, vLLM and Qwen models on DGX Spark, including automated evaluation regression-test suites; video analytics; accelerated development using Claude.
- Responsible for the System-on-Module that won the 2022 Edge AI and Vision Product of the Year award and a 2022 Sacramento Business Journal Innovation Award, plus its commercial and industrial variants.
- Power delivery (multiphase DC-DC, PoE, flyback), SI/PI and thermal for PCIe accelerator cards and modules with PCIe Gen3, USB 3.0, MIPI and LPDDR4, from concept through layout (HDI), bring-up, environmental test, conformal coating and EMC pre-compliance.
- Simulated and measured power networks, high-speed serial links and DDR interfaces in the time and frequency domains (Cadence Sigrity tools, 3D extraction). Reviewed SoC FC-BGA substrates.
- Analysed SoC SystemVerilog as part of system debug; built a Zynq UltraScale+ MPSoC prototype (PetaLinux); analysed competitor systems; ML development and benchmarking in Python.
- Tooling: a Python utility that derives PI requirements from raw power-simulation data using STFT analysis; PowerShell/SKILL release tools for Cadence; VS Code extensions in TypeScript.
- EDA: Cadence suite (DE, Allegro, PowerSI, SystemSI, PowerDC, OptimizePI), LTspice/LTpowerCAD II, SIMetrix/SIMPLIS.

September 2014 – July 2018

Senior Design Engineer · Imagination Technologies / MIPS

Leeds ● FPGA/SoC ● Hardware ● DSP ● Software

Debug and probes team.

- High-performance CPU debug systems on Xilinx 7 Series: AXI, PCIe bus mastering, DDR3, Aurora, XADC analogue capture, embedded Linux (U-Boot, Buildroot).
- FPGA prototyping platforms for IP cores on UltraScale and AWS EC2 F1 (UltraScale+), covering the whole stack from RTL to Linux device driver.
- On-chip instrumentation cores, and software transactors that drove RTL simulation and emulation over TCP/IP (Verilog/C VPI PCIe transactors).

May 2011 – September 2014

Senior Consultant · Red Embedded

Saltaire ● FPGA/SoC ● Hardware ● DSP ● Software

Consultancy across hardware, FPGA and software.

- FPGA broadcast product using Xilinx video IP (3G-SDI, scaler), AXI and embedded Linux (VHDL, C).
- Two FPGA DSP projects with Sagentia, for geophysics and medical applications (Verilog, VHDL, System Generator).
- High-performance PC-based DSP (video processing) for professional broadcast (Python, C++); automated RF testing for powerline comms (Python).

July 2005 – June 2011

Principal Engineer · Pace

Saltaire ● FPGA/SoC ● DSP

Delivered complete FPGA systems for cable headend and transmodulator products.

- High-performance packet classifiers and switches, with DDR interfaces, an on-chip bus and large FIFO structures.

- DOCSIS QPSK/16-QAM burst receiver and J.83 64/256-QAM modulator PHY and MAC layers; Gigabit Ethernet; high-speed inter-FPGA links; embedded MicroBlaze/PowerPC systems; clock-domain crossings.
- Overhauled the group's verification strategy.
- Also a CableCARD (M-Card) interface and a BER instrument for satellite receivers.

June 2002 –
July 2005

Senior Engineer · Comodo

Bradford ● FPGA/SoC ● Cryptography

Front-end design of a 0.18 μm cryptographic SoC (TPM / security token). Designed and integrated an in-house crypto processor (RSA, SHA-1, 3DES, AES, PRNG) with an 8051 CPU, USB, smartcard and LPC interfaces.

October 1998 –
June 2002

Engineer · Pace

Saltaire ● FPGA/SoC ● Hardware

Built Pace's first hard-disk MPEG-2 prototype (PCB, FPGA) and FPGA blocks (DVB, UDMA-66) for a 3DES-protected PVR, which won the company's Most Inspiring Invention award in 2000. Also an ADSL-HPNA set-top-box bridge, and an IrDA handset for speech/speaker recognition.

July 1994 –
August 1997

Hardware Engineer · Thales

Stockport ● FPGA/SoC ● Hardware

Designed the Sonar 2076 data transceiver (1 Gbit/s fibre optics, ECL serial datapath, Fibre Channel, SHARC processors); worked on a DSP co-processor ASIC.

**SELECTED
PUBLIC WORK**

I built these for my own learning, and I am still working my way through them. The full set is in the [portfolio](#).

HW Design-Space Agent

A LangGraph agent that explores hardware design trade-offs from one spec down a fidelity ladder to synthesis, with every number from a recorded run.

[hw-design-space-agent.vercel.app](#)

Signal Integrity & High-Speed Digital Design

Getting a signal from one chip to another intact: transmission lines, return paths, materials, vias, crosstalk, jitter, power integrity, timing budgets, de-embedding and channel operating margin. Every number is computed by a model and checked against published worked examples.

[brendanjameslynskey.github.io/Signal_Integrity](#)

Agent Orchestration Explained

Each of 39 sessions also runs in real LangGraph 1.2.14, and after every one of 71 operations its whole checkpoint history equals the engine's.

[agent-orchestration-explained.vercel.app](#)

Transformer Decoder Explained

The TypeScript transformer in your browser is checked against PyTorch, operation by operation, to within 1e-5, and the animations' frames against a float64 PyTorch run of the same seeded weights.

[transformer-decoder-explained.vercel.app](#)

Systolic Arrays Explained

The cycle-accurate model's output-stationary frames match a SystemVerilog array simulated in Verilator 5.020 on every accumulator after every clock edge: 613 values, 0 mismatches.

[systolic-arrays-explained.vercel.app](#)

FHE Accelerator Simulators

Simulating a fully homomorphic encryption accelerator running CKKS bootstrapping: the workload, the anatomy of bootstrapping, a SimPy accelerator model with a live in-browser simulator, optical NTT engines and the design space.

[brendanjameslynskey.github.io/FHE_Hub_Accelerator_Simulators](#)

EDUCATION

2003–2008

MSc Low Power Systems Integration, University of Manchester (part-time)

2010–2013

Diploma in Mathematics, The Open University (part-time)

1997–1998

MSc Music Technology (DSP), University of York

1991–1994

BEng (Hons) Electronic Engineering, University of Manchester

CERTIFICATIONS

● Xilinx Certified Engineer

● Digital Signal Processing Specialization (and others in DSP)

● MCP Crash Course: Complete Model Context Protocol (and others in AI and MCP)

Selected; full list on LinkedIn.

● Accelerated Computer Science Fundamentals Specialization

● AI Engineer Core Track: LLM Engineering, RAG, QLoRA, Agents

● Cadence: SiP Layout v17.2 exam; Celsius Thermal Solver v2021 exam (and others)